

Method and system of jitter compensation

TECHNICAL FIELD OF THE INVENTION

The present invention relates to sigma-delta modulators, $\Sigma\Delta$ modulators, and phase locked loops. Especially, it re-
5 relates to jitter compensation in $\Sigma\Delta$ -controlled fractional-N frequency synthesizers.

BACKGROUND AND DESCRIPTION OF RELATED ART

Many communications systems require stable and low noise frequency for communication. Exemplary such systems are
10 GSM, DCS 1800 and Bluetooth. Stable frequencies, flexible to various reference oscillator frequencies, can be achieved by a fractional-N synthesizer. A fractional-N synthesizer generates frequencies between two respective nominal frequencies determined from two rationals times a
15 reference frequency. Generally the rationals are achieved by a frequency dividing circuit altering between two integer divisors. By altering between the rationals according to a specified pattern a desired frequency can be achieved for a range of reference oscillators. A problem of alter-
20 ing between frequencies (division ratios) is that phase noise is introduced. The synthesized frequency will comprise a range of frequency components of the output signal being higher or lower than the desired frequency. A $\Sigma\Delta$ -controlled fractional synthesizer according to prior art
25 is shown in figure 1.

U.K. Patent Application GB2097206 illustrates a phase locked loop type frequency synthesizer including a dual switched frequency divider. A compensation signal is generated and adaptively adjusted to reduce phase jitter. The
30 phase jitter is due to the output pulses of the variable

divider not being regularly spaced. In one embodiment the irregularities are suppressed before the signal is applied to the input of the phase comparator.

U.S. Patent US5834987 describes frequency synthesizer systems and methods including a programmable frequency divider. The divider is controlled to divide frequency of a VCO output signal by a first or a second integral ratio. A $\Sigma\Delta$ modulator is responsive to a modulation input to produce the divider control input. A ripple compensation signal is provided to phase detector output.

U.S. Patent US4179670 discloses a fractional division ratio synthesizer with jitter compensation. Jitter compensation is inserted at output of phase comparator. The compensated signal is passed through a loop filter to a voltage-controlled oscillator. A nominal division ratio of M is increased by 1 for a fraction of a number of periods at a reference frequency, f_r . The fraction is a ratio of $N/2^n$, where N may be increased by 1 on a cyclic basis using a $\Sigma\Delta$ modulator clocked at f_r .

U.S. Patent US4771196 describes an electronically variable active analog delay line utilizing cascaded differential transconductance amplifiers with integrating capacitors.

U.S. Patent application US20020008557 presents a digital phase locked loop where the output of a digital controlled oscillator feeds multi-stage tapped delay lines, providing a range of clock signals at different frequencies. A control signal representing timing error in the output signal determines a tap of the tapped delay line for output.

U.S. Patent US5036294 reveals a switched capacitor phase locked loop.

None of the cited documents above discloses a method and system for frequency synthesis providing jitter compensation prior to phase detection or posterior to oscillator signal generation of a phased locked loop, wherein jitter
5 compensation is introduced by means of a variable delay line.

SUMMARY OF THE INVENTION

For phase locked loop frequency synthesizers, fast switching between different frequencies (as e.g. in a High-Rate
10 extension to Bluetooth) requires large loop bandwidths. Prior art phase locked loops with large loop bandwidth generally has too much out-of-band noise in many applications. A substantial part of prior art noise originates from the frequency divider when switching between different divi-
15 sors.

Consequently, it is an object of this invention to provide a method and system of jitter compensation, reducing out-of-band noise stemming from frequency division circuits.

Further, it is an object to reduce such noise/jitter, prior
20 to the jitter being further affected by phase detector nonlinearities.

It is also an object to accomplish jitter compensation by means of variable delay circuitry and delay control circuitry.

25 Another object is to accomplish the delay control by means of a $\Sigma\Delta$ modulator.

Finally, it is also an object to realize the variable delay circuitry by means of a controllable tapped delay line.

These objects are met by the invention controlling a multi-stage tapped delay line.

Preferred embodiments of the invention, by way of examples, are described with reference to the accompanying drawings
5 below.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a $\Sigma\Delta$ -controlled synthesizer according to prior art.

Figure 2 shows a first embodiment of compensation of $\Sigma\Delta$
10 modulator induced jitter according to the invention.

Figure 3 shows the first embodiment of compensation of $\Sigma\Delta$ modulator induced jitter according to the invention with a digital variable delay.

Figure 4 shows a generalized first embodiment of compensation
15 tion of $\Sigma\Delta$ modulator induced jitter according to the invention.

Figure 5 shows a second embodiment of compensation of $\Sigma\Delta$ modulator induced jitter according to the invention.

Figure 6 shows a third embodiment of compensation of $\Sigma\Delta$
20 modulator induced jitter according to the invention.

Figure 7 shows an embodiment of delay control according to the invention.

Figure 8 shows an embodiment of variable delay realized by a tapped delay line according to the invention.

25 Figure 9 shows a first canonical form of variable delay realized by a tapped delay line comprising D flip-flops according to the invention.

Figure 10 shows a second canonical form of variable delay realized by a tapped delay line comprising D flip-flops according to the invention.

Figure 11 illustrates a 50% duty cycle clock frequency signal according to the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

With reference to figure 1, a $\Sigma\Delta$ -controlled synthesizer architecture comprises a phase-frequency detector «PFD», a low-pass loop filter «LPF», a voltage controlled oscillator «VCO» and a frequency divider «Divide by N or N+1». The frequency divider «Divide by N or N+1» is controlled by a $\Sigma\Delta$ modulator « $\Sigma\Delta$ modulator» clocked at frequency f_{ref} with a fractional setting input «fraction». The reference clock signal « f_{ref} » of frequency f_{ref} is input to the phase-frequency detector to be compared with the frequency-divided output signal « f_{out} » of the voltage-controlled oscillator «VCO». By modulating the frequency division factor via the $\Sigma\Delta$ modulator «Div ctrl» an average frequency division factor, N_a , is obtained

$$N \leq N_a \leq N+1.$$

The power spectral density of the frequency division factor is small for low frequencies and increases to a maximum for frequencies around $f_{\text{ref}}/2$, with a $\Sigma\Delta$ modulator clocked at f_{ref} . High frequency components are suppressed by the low-pass loop filter «LPF». However, out-of-band noise level may still be too high for many applications. This is particularly a problem for larger loop-bandwidths. Larger loop-bandwidths are e.g. necessary when fast switching between different frequencies is required, as is the case in e.g. high-rate extensions to Bluetooth.

Some prior art solutions compensate this noise by adding a compensation current at the input of the loop filter. This solution, however, encounters at least two disadvantages:

- 5 - Due to non-linearities in the phase detector the phase noise will be frequency translated from higher frequencies to lower (baseband). Once in baseband it will be difficult, if not impossible, to compensate for the phase noise.
- 10 - For digital implementations of the $\Sigma\Delta$ converters (which are more common than analog $\Sigma\Delta$ converters), an analog digital-analog, D/A, converter is required to convert the compensation signal to an analog current. Requiring one or more D/A converters makes manufacturing proc-
15 essing more complicated.

The invention solves these problems by phase-compensating a signal prior to the signal being input to the phase-frequency detector «PFD».

20 Figure 2 shows a first embodiment of compensation of $\Sigma\Delta$ modulator induced jitter according to the invention.

A variable delay element «Var delay» delays the input signal to the phase detector «PFD» in accordance with a control signal from a control element «Delay calc», calculating the required jitter compensation. Preferably, also the
25 control element is clocked at frequency f_{ref} . The required jitter compensation is determined from signals available from the $\Sigma\Delta$ modulator. The delay-control signal «DCS» is input to the variable delay element «Var delay».

30 The variable delay «Var delay» controls the momentary phase of the signal. Preferably, the controlled quantity is the momentary zero-crossing of the signal fed to the input of

the phase-frequency detector «PFD». The variable delay then controls the zero crossing instances.

With no compensation, as in figure 1, and assuming a locked loop, the time between two zero-crossings, T_d , of the signal «s_{fb}» fed back to detector «PFD» at time nT_{ref} , where n is an integer and $T_{ref}=1/f_{ref}$ could be expressed as

$$T_d(mT_{ref}) = N_a T_{out} + q(mT_{ref}) T_{out} ,$$

where $T_{out}=1/f_{out}$ and $q(nT_{ref})$ is the period jitter.

The accumulated phase jitter at period n , assuming system startup at period 0, then is

$$\Delta\phi(mT_{ref}) = 2\pi f_{ref} T_{out} \sum_{k=0}^m q(kT_{ref}) .$$

The variable delay may be realized entirely digitally as particularly illustrated in figure 3, also illustrating clocking «Clk2» of the digital delay «Dig Delay». Preferably, the digital delay is clocked by the output frequency signal «f_{out}». Both positive and negative flanks of the output frequency signal «f_{out}» can be used to achieve a stepsize as small as $0.5 T_{out}$, for a 50% duty cycle output frequency signal. As in figure 2, the control element «Delay calc» and the $\Sigma\Delta$ modulator « $\Sigma\Delta$ modulator» are preferably clocked «Clk1» by the reference frequency clock signal «f_{ref}».

In a generalized embodiment an average division factor, N_a , is obtained by weighting. Figure 4 illustrates a generalized first embodiment where a range of frequency division factors, $N_i \in \{..., N-1, N, N+1, N+2, ...\}$, are averaged by weighting

$$N_a = \sum_i w_i N_i ,$$

where w_i are weights, such that

$$\sum_i w_i = 1.$$

Similar generalization also applies to the second and third
5 embodiments as would be obvious to the reader.

Figure 5 shows a second embodiment of compensation of $\Sigma\Delta$
modulator induced jitter according to the invention. In
figure 5 the jitter is compensated prior to the dividing
element «Divide by N or N+1». As compared to the preferred
10 embodiment of figure 2 the frequency of the signal input to
the variable delay «Var/dig delay» is much higher. Fur-
ther, the divisor of the division element needs to be com-
pensated for. The delay calculator and the $\Sigma\Delta$ modulator
are clocked «Clk1» by the reference frequency «f_{ref}». The
15 variable delay «Var/dig delay» could be analog or digital.
Preferred embodiments of analog and digital delays accord-
ing to the invention are illustrated in figures 8-10. For
the case of digital delay, the delay elements of variable
delay «Var/dig delay» are preferably clocked by a clock
20 signal «Clk2» identical to the input signal «f_{out}». Conse-
quently, the clock signal could be retrieved internally of
the variable delay «Var/dig delay» without a particular ex-
ternal clock signal input port. For smallest stepsize, the
delay elements of a digital variable delay are preferably
25 triggered by both positive and negative flanks of a 50%
duty cycle clock signal. The clock signal «Clk2» is not
required for an analog variable delay «Var/dig delay».

Figure 6 shows a third embodiment of compensation of $\Sigma\Delta$
modulator induced jitter according to the invention. The

output signal of phase-frequency detector «PFD» depends on the phase difference between its two input signals. This difference is the same whether the phase of the first input is advanced or the phase of the second input is lagged.

5 Consequently, the sign of the variable delay of element «Var/dig delay» is reversed as compared to the embodiment of figure 2. As in figure 5 the delay calculator «Delay calc» and the $\Sigma\Delta$ modulator are clocked «Clk1» by the reference frequency «f_{ref}». The variable delay «Var/dig delay»

10 could be analog or digital. For the case of digital delay, the delay elements are clocked by clock signal «Clk2». Preferably, the output frequency signal «f_{out}» is used for clocking the digital variable delay as in the embodiment of figure 3. Both positive and negative flanks of the out-

15 put frequency signal «f_{out}» can be used to achieve a step-size as small as $0.5 T_{out}$, for a 50% duty cycle output frequency signal. The clock signal input «Clk2» is not required for an analog variable delay «Var/dig delay».

The embodiments of figures 2-6 can be combined. The invention covers, e.g., embodiments with more than one variable

20 delay element.

Figure 7 shows an embodiment of delay control according to the invention. An estimate of the accumulated phase-jitter $\Delta\phi(nT_{ref})$ is obtained by integrating an error signal « ϵ ».

25 The error signal is the difference between the input signal «fraction», corresponding to the desired fraction N_a , and the output signal «Div ctrl» controlling the frequency dividing element «Divide by N or N+1». «Div ctrl» is output from a $\Sigma\Delta$ modulator clocked by clock signal «Clock». Phase

30 is basically integrated frequency and the error signal « ϵ » is integrated and scaled by $2\pi/N_a$ to obtain the estimated phase jitter in «Delay calc». The variable delay and delay

control signal «DCS» corresponds to this estimate for the embodiment of figure 2. Also «Delay calc» is clocked by clock signal «Clock». The delay control signal of the embodiment in figure 5 is N_a times greater, or alternatively
5 the variable delay is scaled accordingly in delay element «Var/dig delay». The delay control signal of the embodiment in figure 6 has a reversed sign or this sign is included in delay element «Var/dig delay».

Figure 8 shows an embodiment of an analog variable delay
10 realized by a tapped delay line according to the invention. The tapped delay line is composed of a number of cascaded segments, each comprising an amplifier, illustrated as an inverter, with transconductance, G_i , a capacitor with capacitance, C_i , and a switch S_i , $i \in [0, n]$, where n is the number of segments of the tapped delay line. The total delay
15 of the tapped delay line equals the sum of delays of segments with closed switches S_i , where segment i with closed switch contributes with a delay proportional to G_i/C_i . Various transconductances G_i can be obtained by varying supply voltage or bias current (depending on the transconductance circuitry).
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A noisy variable delay may itself introduce more phase noise than compensated by the varying delay. For a tapped delay line as illustrated in figure 8, the noise level can
25 be kept at a minimum if powered from a low-noise stabilized supply voltage and by not using more delay than necessary. Deviation from nominal values due to tolerances of manufacturing processes may also call for consideration. For most applications particular low-noise designed inverters are
30 not required. A further advantage of the embodiment of figure 8 in relation to jitter compensation is that a separate multi-bit digital-analog, D/A, converter can be eliminated.

- Given equal transconductances, G_i , for all inverters, the capacitors may represent binary values, i.e. $C_i = 2^i C_0$, $i > 0$. The switches S_i , $i \geq 0$, can then have their binary correspondences (1 for closed switch and 0 for an open switch) in a binary delay control signal. At least this is the case for a desired level of precision as, as explained above, the delay line generated noise increases with number of segments. However, also other alternatives of representing the delay are covered by this invention as well.
- 10 A great advantage of the embodiment of the variable delay as illustrated in figure 8 is that the capacitors can be implemented by gate-bulk capacitances of CMOS transistors. Thereby the variable delay can be implemented in a well known digital CMOS manufacturing process.
- 15 The tapped delay line may also be fully digital as illustrated in figures 9 and 10. The figures show embodiments of variable delay realized by a tapped delay line comprising D flip-flops «D₀», «D₁», «D₂», ..., «D_n». The D flip-flop «D₀» is optional. Each D flip-flop «D₀», ..., «D_n» is clocked by a clock signal «Clock». If the flip-flops are flank-triggered on only one flank (positive or negative) each flip-flop represents a delay stepsize of T_{clock} , where T_{clock} is the time-period of the clock signal «Clock». Preferably, the flip-flops are triggered on both positive and negative flanks of a 50% duty cycle clock signal, illustrated in figure 11, the delay stepsize is reduced to $T_{clock}/2$. In figure 11, a bias level illustrates that the clock frequency signal can be NRZ (no return to zero) or RZ (return to zero). In figures 9 and 10, the switches S_i , $i =$
- 20 0,1,2, ... n, are controlled by the delay control signal. In both figures 9 and 10 only one of the switches «S₀», «S₁», ..., «S_n» are connected at the same time.
- 25
- 30

Figure 9 shows a first canonical form and figure 10 a second canonical form of a fully digital tapped delay line.

The invention is not intended to be limited only to the embodiments described in detail above. Changes and modifications may be made without departing from the invention. It covers all modifications within the scope of the following claims.